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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/934,443	LANDMAN ET AL.	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-6, 9-21 and 23-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The cited claims detail the substantially identical processing programs wherein substantially identical indicates that optional and minor configuration differences **may** exists. The claims do not definitively indicate whether this differences exists or do not exists. Applicant is requested to either claim the differences or remove the limitation.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 15-17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The cited claims are directed to a non-functional data structure stored in a computer readable medium. M.P.E. P. 2106 details that such non-functional data structures are non-statutory even if claimed in a computer medium. The claims also detail an intended use of the data. The intended use of the data structure cannot be used to make a claim statutory. The cited claims should be

either 1) a system comprising the cited processing elements and the data structure such that the data structure is submitted to the different processing elements as detailed in the claims or 2) a computer medium having both the data structure and code for submitted the parameter data of the data structure to separate non-threaded sets of executable instructions...".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 9-11, 13-15, 17, 18, 21, 23, 25-27 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by PASSERA (U.S. Patent 6,415,286).

As to claim 1, PASSERA teaches an apparatus, implemented in a computer medium, for subdividing input data (data space) associated with a software program and processing each subdivided input data (sub-region of the data space) on one or more processing elements (processors / slave processors), comprising: a non-threaded initiating program; one or more non-threaded processing programs (ApplyModel Slave), wherein each of the one or more non-threaded processing programs are substantially identical and perform the same functions or operations as remaining ones of the one or

more non-threaded processing programs, wherein substantially identical indicates that optional and minor configuration differences may exists (each slave is an instance of the Master that is executed on the slave processor to perform a computation with the data set); and a wrapper that intercepts a call to the initiating program and operable to subdivide input parameters into one or more job quanta (master subdivides data space into sub-regions to be distributed to slave processors), wherein each job quantum is submitted for execution to a separate processing program (slave instance) selected from the one or more processing programs residing on a separate processing element (slave processor) (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 11, reference is made to a method that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above.

As to claim 15, PASSERA teaches a job quanta data structure implemented in a computer readable medium, comprising: a first data (sub region of data space); a second data (sub-region of data space) wherein the first and second data are to be delineated (partitioned along at least one plane orthonogonal to a determined axis) and independently submitted as input parameter data for execution by separate non-threaded sets of executable instructions (slave instances) and processed in parallel on different processing elements (slave processors), wherein each separate non-threaded set of executable instructions is substantially identical and performs the same functions

as remaining ones of the non-threaded sets of executable instructions, wherein substantially identical indicates that minor configuration differences may exist (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 18, reference is made to a system that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above. Claim 18, further details means for executing the software program and the separate software programs in parallel. PASSERA teaches executing the software programs in parallel (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 21, reference is made to a method that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above.

As to claim 23, reference is made to a method that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above.

As to claim 27, reference is made to a system that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above. Claim 27 further details the job quantum's are processed in parallel. PASSERA teaches the job quantum's are processed in parallel (see abstract; col. 3, lines 21-63; col. 5, line 56 –

col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 9, PASSERA teaches that at least one of the processing elements reside in a disparate processing environment (col. 13, lines 5-12).

As to claim 10, PASSERA teaches the input parameters are normalized prior to being subdivided into the job quanta (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 13, PASSERA teaches submitting at least one job quantum for execution to the first set of executable instructions (slave instance) (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 14, PASSERA teaches the executions occur in parallel (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 17, PASSERA teaches the first and second data are initially submitted as input parameter data to a single instruction set (see abstract; col. 3, lines

21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 25, PASSERA teaches the executions occur in parallel (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51).

As to claim 26, refer to claim 1 for rejection.

As to claim 29, PASSERA teaches that at least one of the processing elements reside in a disparate processing environment (col. 13, lines 5-12).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 3, 12, 19, 20, 22, 24, 28 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over PASSERA (U.S. Patent 6,415,286) in view of REHG (U.S. Patent 6,480,876).

As to claim 22, reference is made to a system that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above. Claim 22, further

details a network, memory operatively coupled to a plurality of processing elements and recombining output data from the processing elements. PASSERA teaches a network and memory operatively coupled to the plurality of processing elements (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51). However, PASSERA does not teach recombining the output data.

REHG teaches a parallel distributed system wherein a scheduler (controller) that receives the plurality of job quanta from the wrapper (data parallel partitions) and submits substantially in parallel different job quantum associated with the job quanta to a number of software programs (data parallel threads / tasks / worker tasks) for processing, wherein the scheduler selects the number of software programs based on processing loads (performance / performance goal) associated with the number of software programs and recombines the output data from the processing elements (col. 11, line 43 – col. 12, line 32; col. 7, line 1-38; col. 7, line 56 – col. 8, line 61). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of PASSERA with the teachings of REHG in order to facilitate data parallelism for dynamic applications wherein the applications include one or more tasks or processing threads (col. 4, lines 62-65).

As to claim 30, reference is made to a system that corresponds to the apparatus of claim 1 and is therefore met by the rejection of claim 1 above. Claim 30 further details a scheduler that receives the plurality of job quanta from the wrapper and

submits substantially in parallel different job quantum associated with the job quanta to a number of software programs for processing, wherein the scheduler selects the number of software programs based on processing loads associated with the number of software programs. However, PASSERA does not teach the scheduler selecting the number of software programs based on processing loads.

REHG teaches a parallel distributed system wherein a scheduler (controller) that receives the plurality of job quanta from the wrapper (data parallel partitions) and submits substantially in parallel different job quantum associated with the job quanta to a number of software programs (data parallel threads / tasks / worker tasks) for processing, wherein the scheduler selects the number of software programs based on processing loads (performance / performance goal) associated with the number of software programs (col. 11, line 43 – col. 12, line 32; col. 7, line 1-38; col. 7, line 56 – col. 8, line 61). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of PASSERA with the teachings of REHG in order to facilitate data parallelism for dynamic applications wherein the applications include one or more tasks or processing threads (col. 4, lines 62-65).

As to claim 2, refer to claim 22 for rejection.

As to claim 3, PASSERA does not teach the scheduler selecing the number of software programs based on processing loads.

REHG teaches a parallel distributed system wherein a scheduler (controller) that receives the plurality of job quanta from the wrapper (data parallel partitions) and submits substantially in parallel different job quantum associated with the job quanta to a number of software programs (data parallel threads / tasks / worker tasks) for processing, wherein the scheduler selects the number of software programs based on processing loads (performance / performance goal) associated with the number of software programs (col. 11, line 43 – col. 12, line 32; col. 7, line 1-38; col. 7, line 56 – col. 8, line 61). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of PASSERA with the teachings of REHG in order to facilitate data parallelism for dynamic applications wherein the applications include one or more tasks or processing threads (col. 4, lines 62-65).

As to claim 12, refer to claim 22 for rejection.

As to claim 19, refer to claim 22 for rejection.

As to claim 20, REHG teaches means for trapping and reporting error conditions generated by the execution of the software programs (via observing the effect on the application and system states) (col. 11, line 43 – col. 12, line 33). Therefore, it would be obvious to one of ordinary skill in the art to combine the teachings of PASSERA with the teachings of REHG in order to facilitate data parallelism for dynamic applications

wherein the applications include one or more tasks or processing threads (col. 4, lines 62-65).

As to claim 24, refer to claim 22 for rejection.

As to claim 28, refer to claim 22 for rejection.

As to claim 31, refer to claim 22 for rejection.

As to claim 32, refer to claim 20 for rejection.

8. Claims 4-6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over PASSERA (U.S. Patent 6,415,286).

As to claim 4, PASSERA teaches that a processor can act as both a master and a slave. Therefore, it would be obvious to the teachings of PASSERA that the distributing of data spaces among slave instances functions at all computers since a processor can act as both a master and a slave and therefore each processor has a wrapper.

As to claims 5 and 6, PASSERA teaches the processing programs are identical instances of one another and perform a computation operation (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11,

line 25; col. 13, lines 5-25; col. 14, lines 15-51). It would be inherent to the teachings of PASSERA that since the programs are instances of one another the operations are obviously identical. However, PASSERA does not teach that the operations are bioinformatics calculations. Official Notice is taken in that such operations are well known in the art and therefore would be obvious in view of PASSERA that the computation operation is a bioinformatics operation.

As to claim 16, PASSERA teaches the data are delineated (see abstract; col. 3, lines 21-63; col. 5, line 56 – col. 6, line 43; col. 9, lines 10-59; col. 10, line 11 – col. 11, line 25; col. 13, lines 5-25; col. 14, lines 15-51). However, PASSERA does not teach that the delineating is performed in XML. Official Notice is taken in that XML is a well known language that allows symbols indicating a delineating of code and therefore would be obvious in view of PASSERA in order to determine where the data should be separate at.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 29, 2006

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER